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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,830	03/29/2004	Robert Bergmann	E0196.0006	3112

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EXAMINER	
ABOAGYE, MICHAEL	

ART UNIT	PAPER NUMBER
1725	

MAIL DATE	DELIVERY MODE
09/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,830	BERGMANN ET AL.	
	Examiner	Art Unit	
	Michael Aboagye	1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/25/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,2,4,5 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka et al. (US Patent No. 5,668,058) in view of Yoshida et al. (US Patent No. 5,305,944)

Tanioka et al. teaches device for soldering contacts on vertically integrated semiconductor chips, comprising: a clamping device that receives and transports a circuit board having components (note, Tanioka on column 4, line 50 teaches mounting the circuit board on the bonding stage 7, figure 10C, The examiner interprets mounting as clamping, hence said device is necessarily equipped with a clamp or a fastening means to hold the circuit board "3" in position on the bonding stage in alignment with the bonding tool. Tanioka et al. also teaches a set up wherein the circuit board is transported by a conveyor and aligned beneath the chip mounting head, (23, figure 3 and column 2, lines 65-67) a flushing device including a plate with a window (see, the examiner interprets features 9, the gas source and the cover 8 combined as the flushing device since these features combined supply and provide confined space for the inert gas, the

aperture between the two plates to receive the bonding tool is considered by the examiner as the window, see figure 10C), a first and a second gas channels (see, the feature 9 within both edges of the cover (8) and a first and second gas outlet opening arranged at the two edges of the cover and between said edges and in the window area around the tool (9, figure 10C), note that these openings provide exit way to expel gases from the space defined within the cover and the stage area), the plate being aligned parallel to a stage (7), (It should be noted that in the conveyor system the bonding stage is parallel to the housing (28) (in figure 6, the partition 28 which maintains the nonoxidizable atmosphere being aligned parallel to the conveyor including the bonding stage); a chip mount arranged above the clamping device over the window such that a chip is held on a side or the planar area of the chip mount facing the clamping device and vertically moved over the and pressing chip to mount on the printed circuit board (6, figure 10C); and infra red heater that heats a chip held on the chip mount to reflow the solder (column 4, lines 14-16

Tanioka et al. teaches heating means including an infrared radiation source but fail to teach a heater that heats the chip on the chip mount from the side of the chip facing the chip mount.

Yoshida et al. teaches a bonding apparatus comprising a chip press mechanism (300) having an associated plate member (301) for pressing the chip (2) onto the substrate (22) and bonding the chip to the substrate by the solder bump (3) disposed beneath the chip (see figures 12 and 13). (Note the chip press mechanism and the associated plate member are operable in mounting or

clamping the chip onto the substrates hence the examiner interprets these two composite features as functionally equivalent to the chip-mounting device). An infrared device (210, figures 12 and 13) illuminates radiant heat through the plate member to the chip from a side of the chip facing the chip mount and heating to melt the solder bump (3) (note, the plate member is transmittable and therefore permeable to infrared light), (see, Yoshida et al., column 7, lines 21-39 and column 9, lines 41-65). Yoshida et al. also teaches the benefits of having a an infrared –light- transmittable or absorbable material, said benefits including minimizing temperature rise due to reflection of the infrared beam and thereby preventing excessive heating of the chip (Yoshida et al., column 10, lines 18-29). Yoshida et al. also teaches a device having a heating source including either a xenon lamp, a halogen lamp or a laser source (see, Yoshida et al., column 8, lines 4-9). Yoshida et al. further teaches a device including a converging optical system including reflective mirror fro converging the infrared light beam onto the bumps to be heated and also allowing selective heating to be conducted (see, Yoshida et al., column 3, lines 27-36, column 8, lines 16-25 and lines 52-58).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to use in the device of Tanioka et al. an infrared transmittable chip mount as taught by Yoshida et al. to minimize temperature rise due to reflection of the infrared beam and thereby preventing excessive heating of the chip (Yoshida et al., column 10, lines 18-29).

3. Claims 6-8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka et al. (US Patent No. 5,668,058) in view Yoshida et al. (US Patent No. 5,305,944) as applied to claims 1 and 13 and further in view of Tsumura et al. (US Patent No. 6,288,376).

Tanioka et al. and Yoshida et al. fail to teach an induction-heating source.

However Tsumura et al. discloses a method and device for melting a bump with a heater comprising an induction coil; an electrically conducting coil fitted into the solder so that the solder can be heated by an induction of eddy currents and causing the solder to melt (Tsumura et al., column 6, lines 32-41); said heating process requires no flux application, cleaning or drying resulting in enhanced bond integrity (Tsumura et al., abstract, column 2, lines 21-27).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to have used an induction-heating source in the combined invention of Tanioka et al. and Yoshida et al. as taught by Tsumura et al. in order to ensure a clean solder melting process and achieving a bond with enhanced integrity (Tsumura et al., abstract, column 2, lines 21-27).

4. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka et al. (US Patent No. 5,668,058) in view of Yoshida et al. (US Patent No. 5,305,944) and of Xie et al. (US Patent No. 6,334,567)

Tanioka et al. teaches a method for soldering a chip to a circuit board, comprising: applying a solder to contact the chip and the circuit board; exposing the solder to a forming gas by using a flushing device including a plate with a

window (see, figure 10C and 10D and column 4, lines 40-65); heating the solder with an infrared heater that heats a chip held on the chip mount, melting the solder (Tanioka et al., column 4, lines 14-16) and pressing the chip to be joined to the printed circuit board (6, figure 10C). (Note, the examiner interprets features 9, the gas source and the cover 8 combined as the flushing device since these features combined supply and provide confined space for the inert gas).

Tanioka et al. teaches heating means including an infrared radiation source but fail to teach a heating the chip through the chip mount from the side of the chip facing the chip mount.

Yoshida et al. teaches bonding method comprising a chip press mechanism (300) having an associated plate member (301) for pressing the chip (2) onto the substrate (22) and bonding the chip to the substrate by the solder bump (3) disposed beneath the chip (see figures 12 and 13). (Note the chip press mechanism and the associated plate member are operable in mounting or clamping the chip onto the substrates hence the examiner interprets these two composite features as functionally equivalent to the chip-mounting device). Illuminating radiant heat from an infrared device (210, figures 12 and 13), transmitting the radiant beam through the plate member to the chip from a side of the chip facing the plate member and heating to melt the solder bump (3) (note, the plate member is transmittable and therefore permeable to infrared light), (see, Yoshida et al., column 7, lines 21-39 and column 9, lines 41-65). Yoshida et al. also teaches the benefits of having a an infrared –light- transmittable or absorbable material, said benefits including minimizing temperature rise due to

reflection of the infrared beam and thereby preventing excessive heating of the chip (Yoshida et al., column 10, lines 18-29). Yoshida et al. also teaches a device having a heating source including either a xenon lamp, a halogen lamp or a laser source (see, Yoshida et al., column 8, lines 4-9). Yoshida et al. further teaches a device including a converging optical system including reflective mirror fro converging the infrared light beam onto the bumps to be heated and also allowing selective heating to be conducted (see, Yoshida et al., column 3, lines 27-36, column 8, lines 16-25 and lines 52-58).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to use an infrared transmittable chip mount to direct heat to the back side of the chip in the method of Tanioka et al. as taught by Yoshida et al. to minimize temperature rise due to reflection of the infrared beam and thereby preventing excessive heating of the chip (Yoshida et al., column 10, lines 18-29).

Tanioka et al. and Yoshida et al. do not expressly teach isothermal solidification.

However, Xie et al. teaches a soldering method for bonding together electronic components by heating and cooling the solder such that the solder undergoes isothermal solidification to forms a layer of a thickness 3-7 microns (Xie et al., abstract, column 1, lines 61- column 2, line 24; column 4, lines 49-56 and figure 1 &2).

It would have been obvious to one of ordinary skill in the art at the time the applicants invention was made to use isothermal solidification in the combined

soldering method of Tanioka et al. and Yoshida et al. as taught by Xie et al. since by isothermal solidification thin solder layer can be used, and therefore, thinner micro components can be assembled (Xie et al., column 1, lines 5-8 and column 4, lines 49-56).

Response to Arguments

5. The examiner acknowledges the applicants' amendment received by USPTO on July 25, 2007. New claims 13-17 have been added, claim 3 has been cancelled therefore claims 1, 2 and 4-17 currently remain under consideration in the application.

6. Applicant's arguments with respect to claims 1, 2 and 4-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wong (US 6,384,366), Baker et al. (US 5,364,011), Kodama et al. (US 5,878,942), Shaw (US 5,430,567) and Schultz et al. (US 4,099,660) are also cited in PTO-892.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Aboagye whose telephone number is

571-272-8165. The examiner can normally be reached on Mon - Fri 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jonathan Johnson can be reached on 571-272-1177. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JONATHAN JOHNSON
PRIMARY EXAMINER

Michael Aboagye
Assistant Examiner
Art Unit 1725
09/05/2007

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